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Letter

Nb-Doped La_2O_3 as Charge-Trapping Layer for Nonvolatile Memory Applications

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***Abstract*—Charge-trapping properties of Nb-doped La_2O_3 (LaNbO) are investigated using an $Al/Al_2O_3/LaNbO/SiO_2/Si$ structure. Compared with the memory device with La_2O_3, the one with LaNbO shows better charge-trapping characteristics, including larger memory window (6.0 V at $\pm$16 V sweeping voltage), higher programming speed (9.1 V at $+$16 V for 1 ms), and better retention property (94% charge retained after 10^4 s at 120 °C), due to its higher trapping efficiency resulted from increased trap density and suppressed formation of a silicate interlayer at the LaNbO/SiO_2 interface by the Nb doping. Therefore, LaNbO is a promising candidate as the charge-trapping layer for nonvolatile memory applications.**

***Index Terms*—Nonvolatile memory, charge-trapping, Nb-doped La_2O_3 (LaNbO), high-k dielectric.**

I. Introduction

METAL-oxide-nitride-oxide-silicon (MONOS)-type flash memories with discrete traps in the nitride dielectric as charge-trapping medium show stronger scaling ability and higher reliability than the floating-gate type memories. Si_3N_4 was the first dielectric as charge-trapping material for MONOS devices. However, the small conduction-band offset relative to SiO_2 and low k value of Si_3N_4 ($k \sim 7$) draw many researchers' interest in investigating suitable high-k dielectrics to substitute Si_3N_4. Among various high-k dielectrics, La_2O_3 seems to be a promising candidate due to its high dielectric constant ($k \sim 25$) [1]. However, La_2O_3 cannot provide a large memory window due to its low trap density [1]–[4] and it is also well-known to easily react with SiO_2 tunneling oxide [5], [6]. Niobium (Nb) oxide has a higher k value ($k \sim 40$) [7], and therefore doping Nb into La_2O_3 can increase its k value. Moreover, Nb doping into La_2O_3 is expected to increase its trap density and suppress its reaction with the SiO_2 tunneling oxide [5], [6]. In this work, based on MONOS capacitors, the charge-trapping characteristics of La_2O_3 with and without niobium doping are studied.

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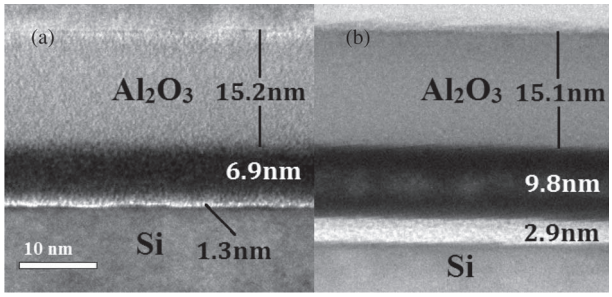

Fig. 1. TEM cross-sectional images of (a) the LaO sample and (b) the LaNbO sample (same scale for both samples).

II. Experiment

MONOS capacitors were fabricated on p-type silicon substrate. After the standard RCA (Radio Corporation of America) cleaning, 3-nm SiO_2 tunneling layer (TL) was grown on the substrate by thermal dry oxidation at 900 °C for 180 s. Then, LaNbO with different contents of niobium was deposited on the wafer by co-sputtering of La_2O_3 and Nb targets in a mixed ambient ($Ar/O_2 = 24/3$). The power of La_2O_3 was fixed at 40 W, while Nb was set as 0 W and 10 W to produce samples with various Nb contents, and denoted as LaO and LaNbO samples respectively. Following that, 15-nm Al_2O_3 blocking layer (BL) was deposited by atomic layer deposition using $Al(CH_3)_3$ and H_2O as precursors at 300 °C. Then, both samples received post-deposition annealing at 900 °C in N_2 for 30 s. This high-temperature annealing was used to account for the thermal treatment for activating the source and drain of memory transistors. Subsequently, aluminum was evaporated and patterned as electrodes. Finally, the samples received forming-gas annealing for 20 minutes at 300 °C. The thickness of the dielectric films and the formation of interlayer at the CTL/SiO_2 interface were determined by cross-sectional transmission electron microscopy (TEM). The elements and their concentration in each layer were determined by secondary ion mass spectroscopy (SIMS). The electrical characteristics of the memory devices were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer.

III. Results and Discussion

Fig. 1 shows the TEM cross-sectional images of the two MONOS capacitors after going through all the processing steps. It is clear that an interlayer forms at the La_2O_3/SiO_2 interface of the LaO sample but not the LaNbO one. Moreover, the TL of the LaO sample becomes much thinner than that of the LaNbO sample, although they were simultaneously formed under the same processing conditions. This is because La_2O_3 can easily react with the SiO_2 TL to form silicate, thus consuming some of the SiO_2 TL [5], [6]. The absence of SiO_2 consumption in the LaNbO sample indicates that Nb doping suppresses La oxide's scavenging behavior towards SiO_2 and thus helps to maintain the desired TL. It should be noted that although an interlayer could be formed at the Al/Al_2O_3 interface, it should have the same influence on the properties of both samples.

Fig. 2 shows the SIMS depth profile of the two samples after going through all the processing steps. In Fig. 2(a), the La content displays two local peaks and one of them overlaps with the peak of SiO_2, suggesting that La diffuses into the TL. In Fig. 2(b), La and Nb display only one peak farther away from the TL, indicating the suppression

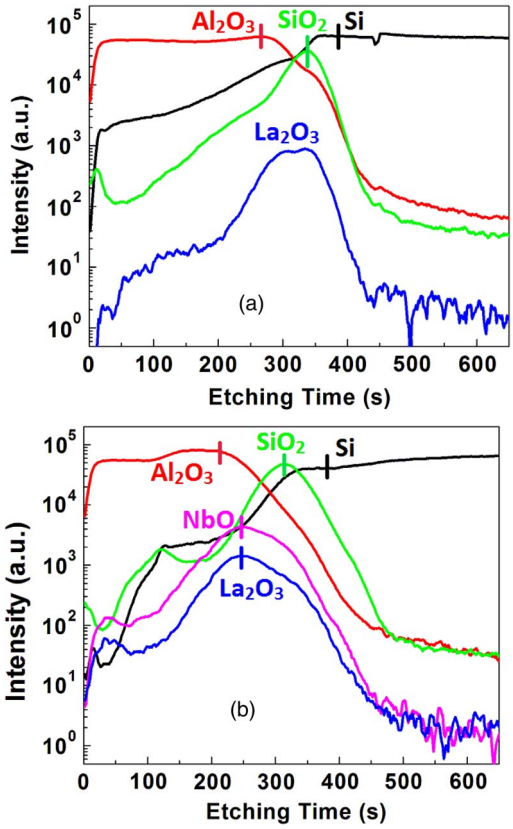

Fig. 2. SIMS depth profile of (a) the LaO sample and (b) LaNbO sample. The Al electrode was removed before SIMS test.

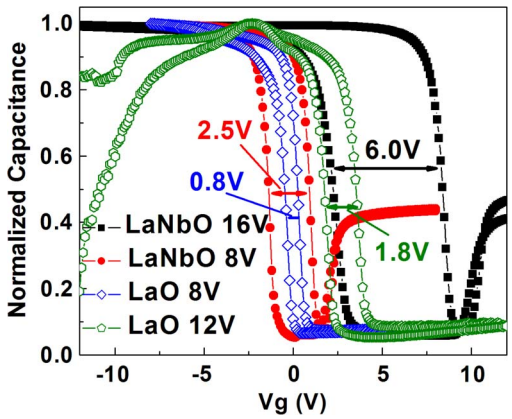

Fig. 3. Hysteresis curves of the LaO and LaNbO samples. Note that both samples have similar equivalent oxide thickness (13.6 nm for LaO and 12.5 nm for LaNbO), and thus similar electric field under the same gate voltage.

of La_2O_3 diffusion by the Nb doping. The quality of the interface between the CTL and TL is improved by the Nb doping, because the suppression of La_2O_3 diffusion protects the interface from the formation of poor-quality silicate interlayer, which is consistent with the TEM results in Fig. 1.

Fig. 3 shows the 1-MHz hysteresis characteristics of the MONOS capacitors under various sweeping voltages. The equivalent oxide thickness (EOT) of the two samples is calculated by:

$$EOT = T\left(\frac{\varepsilon_{SiO_2}}{K}\right) \tag{1}$$

where T is the total physical thickness of the TL, CTL and BL; ε_{SiO2} is the dielectric constant of SiO_2; and K is the equivalent

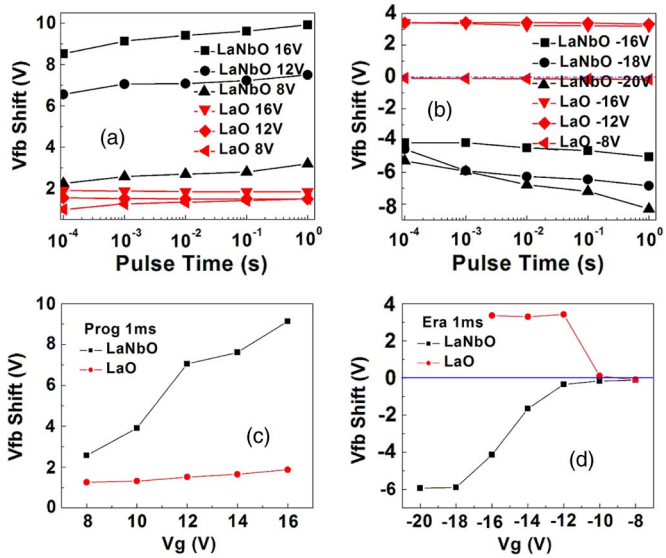

Fig. 4. (a) Program and (b) erase transient characteristics of the LaO and LaNbO samples. (c) Program and (d) erase characteristics of the LaO and LaNbO samples at various operating voltages with a fixed pulse of 1 ms.

dielectric constant of the TL, CTL and BL calculated from the measured capacitance of the samples. Sweep starts from inversion region to accumulation region, and back to inversion region again. For the LaNbO sample, as the sweeping voltage increases from ± 8 V to ± 16 V, the memory window increases from 2.5 V to 6.0 V. On the contrary, the memory window of the LaO sample is only 0.8 V at ± 8 V sweeping voltage, which is much smaller than that of the LaNbO one. The much larger memory window of the LaNbO sample indicates that niobium doping increases the trap density of the charge trapping layer (CTL), thus increasing its charge-trapping efficiency. Moreover, the LaNbO sample can endure higher voltage up to $+16$ V, while the LaO sample breaks down at 12 V as shown in Fig. 3 mainly due to the thinner SiO_2 TL and the silicate interlayer of low quality in the LaO sample (shown in Fig. 1). Another phenomenon worth mentioning is that the initial V_{FB} of both samples increases with increasing sweeping voltage. It is due to electron injection from the gate to the CTL in the accumulation region, which is consistent with the results in Fig. 4 and will be explained in detail later.

Fig. 4 shows the program/erase (P/E) characteristics of the MONOS capacitors. The LaNbO sample always displays much larger V_{FB} shift than the LaO one under the same operating conditions. It is worth emphasizing that the V_{FB} shift of the LaNbO sample is larger even when the sample has thicker TL (shown in Fig. 1), which results in longer distance for charges to tunnel from the substrate through the TL to the CTL. The reason for the larger V_{FB} shift is that the LaNbO sample has higher charge trap density, which is consistent with the conclusion drawn from Fig. 3. The higher trap density in the LaNbO sample can accommodate more charges, leading to larger V_{FB} shift. In addition, the V_{FB} shift of the LaO device hardly increases with increasing positive gate voltage, while that of the LaNbO one does not have the saturation phenomenon and increases significantly with the gate voltage. This phenomenon further confirms the high trap density of the LaNbO sample, indicating that Nb incorporation in La_2O_3 helps overcome the trap deficiency problem of the La oxide. The charge-trap density (N_t) can be estimated by assuming that the trapped-charge centroid is located at the center of the CTL [8], [9]:

$$N_t = \frac{\Delta V_{FB}}{q}\left(\frac{T_{BL}}{\varepsilon_0 \varepsilon_{BL}} + \frac{T_{CT}}{2\varepsilon_0 \varepsilon_{CT}}\right)^{-1} \tag{2}$$

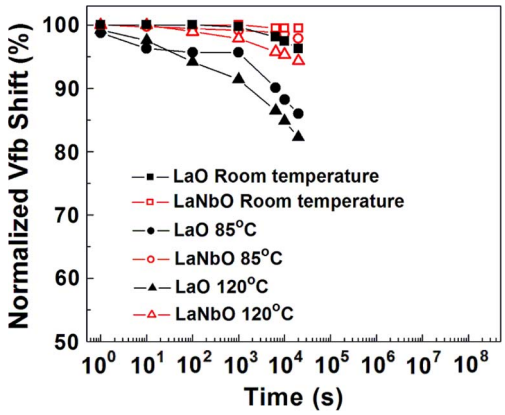

Fig. 5. Retention characteristics of the LaO and LaNbO samples at room temperature, 85 °C and 120 °C.

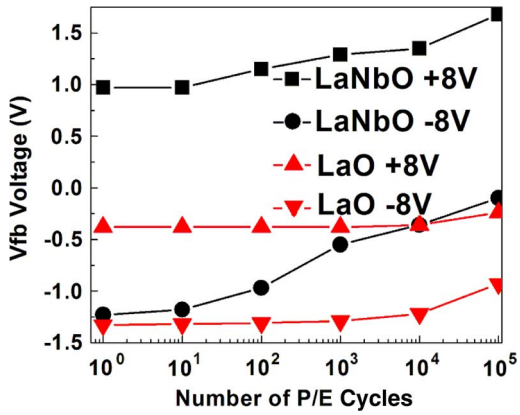

Fig. 6. Endurance characteristics of the LaO and LaNbO samples under ±8-V 100-μs stress pulses at room temperature.

where ΔV_{FB} is the V_{FB} shift with respect to the fresh VFB, q the elementary charge, ε_0 the permittivity of vacuum, T_{BL} and ε_{BL} the thickness and dielectric constant of the BL respectively, T_{CT} and ε_{CT} the thickness and dielectric constant of the CTL respectively. N_t of the LaNbO sample under $\pm 12-$ V sweeping is calculated to be 1.91×10^{13} cm^{-2}, which is much higher than the value $(3.56 \times 10^{12}$ cm$^{-2})$ for the LaO sample. Furthermore, by erasing at -16 V for 1 ms, the LaNbO sample has a V_{FB} shift of -4.1 V, while the LaO one has a positive shift of 3.3 V and shows normal erasing behavior only at -8 V with a small shift of -0.1 V. This abnormal positive V_{FB} shift of the LaO sample is the result of undesirable electron tunneling from the gate to the CTL, which is called erase saturation [10]. It indicates a nonideal CTL/BL interface, which is an important problem to be solved in enhancing the erasing function of memory devices [11], [12]. For comparison, the abnormal positive shift does not exist in the LaNbO sample due to high trap density. The moving electrons during erasing can be divided into two parts: some escape from the CTL through the TL to the substrate, while others flow into the CTL from the gate electrode. For the LaNbO sample with a large number of traps in the CTL, the former outnumber the latter so that the erase saturation is partially overcome. The overall dynamic equilibrium is a normal erasing behavior with a negative V_{FB} shift. Besides the trap density, the quality of the CTL/BL interface also affects the electron flow from the gate to the CTL. The Nb doping can improve the quality of CTL/BL interface and therefore suppress the undesirable electron flow. Additionally, the electrons injected from the gate to the CTL are also responsible for the different initial V_{FB} under different sweeping voltages in Fig. 3 mentioned above. In the accumulation region, the electrons affecting the V_{FB} can be similarly divided into the above two parts. The second part of electrons makes the V_{FB} unable to shift back to its original value.

Fig. 5 shows the retention characteristics of the MONOS samples at three temperatures, with both samples prepared at 10 -V for 1 s. For the LaNbO sample, retention is hardly dependent on testing temperatures, suggesting that thermionic emission plays an insignificant role in the decrease of V_{FB} shift for the LaNbO sample. The good data retention even at high temperature (94% charge retained at 120 °C after 10^4 s) suggests that Nb-doped La_2O_3 is a promising CT material for high-temperature applications. For the LaNbO sample, the dominant reason for the decrease of V_{FB} shift with increasing time is that the electrons stored in the traps in the CTL continuously tunnel back to the substrate. In addition, the annihilation of trapped electrons by the holes may also be responsible for the retention degradation, but it should not be the main degradation mechanism for the LaNbO sample due to few hole traps. The few hole traps can be demonstrated in Figs. 3 and 4 which display no over-erase phenomenon. The reason for the better retention of the LaNbO sample at all the testing temperature should be the thicker and interlayer-free TL in the LaNbO sample (shown in Fig. 1), which is a result of suppressed reaction between SiO_2 and La_2O_3 achieved by the Nb doping. It is worth mentioning that 96% of charge retained is higher than those for other CT materials reported recently: e.g. 70% for nitrided La_2O_3 [1], 85% for Mo-doped La_2O_3 [13], 85% for Ge nitride [14], $<$ 50% for HfO_2/Al_2O_3 [15].

Fig. 6 shows the endurance characteristics of the LaO and LaNbO samples. The initial P/E window of the LaO sample and the LaNbO sample is 0.95 V and 2.2 V respectively. After a 105-cycle P/E stressing, the window degrades to 0.69 V and 1.8 V, corresponding to 27.4% and 19.1% degradation respectively. The smaller degradation of the LaNbO sample suggests that it has stronger resistance against the stress. The degradation of the window is due to the trapped charges remaining at the TL/CTL interlayer (shown in Fig. 1) generated by stressing operation. The low-quality interlayer contains many defects, which act as charge traps. These defects are different from the normal traps in the CTL because charges trapped in the interlayer can leak out easily. As a result, the interlayer defects not only cannot increase the P/E windows, but also provide leaking paths, which are harmful to charge retention (Fig. 5). Moreover, these defects can trap charges in short periods and thus lead to the decreases of the windows [16], [17]. Note the smaller degradation of the window for the LaNbO sample should be ascribed to its interlayer-free TL with fewer defects. It is observed that the LaNbO sample suffers from an upward V_{FB} shift with increasing P/E cycles. This is due to deep-level traps in the LaNbO sample. Electrons trapped in the deep-level traps are more difficult to remove under erasing operation than those in the shallow-level traps. Consequently, with increasing P/E cycles, the number of electrons in the deep-level traps continuously increases, shifting the V_{FB} upward. Although deep-level traps are helpful for programming operation, they are harmful for erasing operation, and thus a trade-off between these two operations is necessary.

IV. Conclusion

The charge-trapping properties of La_2O_3 with and without Nb doping have been investigated based on MONOS capacitor. The memory device with Nb-doped La_2O_3 as CTL shows better characteristics than that with La_2O_3 in terms of memory window, P/E speed, endurance and data retention, which are resulted from higher trap density in CTL and better TL/CTL interface (both induced by the Nb doping). Therefore, Nb-doped La_2O_3 is a promising candidate as CTL for high-performance nonvolatile memory applications.

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